What is claimed:

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1. An arbiter device for a multi-port memory equipped with a first port and a second port, comprising:

an identical address detection device,

wherein the identical address detection device determines whether an input address to the first port and an input address to the second port are identical;

an operation stopping device,

wherein the operation stopping device stops operation of the second port of the multi-port memory when the identical address detection device determines that the input address to the first port and the input address to the second port are identical; and

a selector device,

wherein the selector device selects data and outputs data on the first port of the multi-port memory when the identical address detection device determines that the input address to the first port and the input address to the second port are identical.

2. An arbiter device according to claim 1, wherein the selector device selects data and outputs data on the second port of the multi-port memory when the identical address detection device determines that the input address to the first port and the input address to the second port are not identical.

3. An arbiter device according to claim 1, wherein identical address detection device is responsive to at least one of the input address to the first port and the input address to the second port.

4. An arbiter device according to claim 1, wherein identical address detection device is adapted to generate an identical address detection signal if the input address to the first port and the input address to the second port are identical.

5. An arbiter device according to claim 1, wherein the selector device is responsive to at least one of a data output signal of the first port, a data output signal of the second port, and a buffer output signal.

6. An arbiter device according to claim 1, wherein the selector device is adapted to generate a data output signal.

7. An arbiter device according to claim 1, wherein the arbiter device arbitrates between accesses to the first port and the second port.

8. An arbiter device for a multi-port memory equipped with a write-only first port and a read-only second port, comprising:

an identical address detection device,

wherein the identical address detection device determines whether an input address to the write-only first port and an input address to the read-only second port are identical;

an operation stopping device,

wherein the operation stopping device stops operation of the read-only second port of the multi-port memory when the identical address detection device determines that the input address to the write-only first port and the input address to the read-only second port are identical; and

a selector device,

wherein the selector device selects data and outputs data on the write-only first port of the multi-port memory when the identical address detection device determines that the input address to the write-only first port and the input address to the read-only second port are identical.

9. An arbiter device according to claim 8, wherein the selector device selects data and outputs data on the read-only second port of the multi-port memory when the identical address detection device determines that the input address to the write-only first port and the input address to the read-only second port are not identical.

10. An arbiter device according to claim 8, wherein identical address detection device is responsive to at least one of the input address to the write-only first port and the input address to the read-only second port.

11. An arbiter device according to claim 8, wherein identical address detection device is adapted to generate an identical address detection signal if the input address to the write-only first port and the input address to the read-only second port are identical.

12. An arbiter device according to claim 8, wherein the selector device is responsive to at least one of a data output signal of the write-only first port, a data output signal of the read-only second port, and a buffer output signal.

13. An arbiter device according to claim 8, wherein the selector device is adapted to generate a data output signal.

14. An arbiter device according to claim 8, wherein the arbiter device arbitrates between accesses to the write-only first port and the read-only second port.

15. An arbiter device for a multi-port memory equipped with a readable and writeable first port and a read-only second port, comprising:

an identical address detection device,

wherein the identical address detection device determines whether an input address to the readable and writeable first port and an input address to the read-only second port are identical, and a writing operation to the first port is enabled;

an operation stopping device,

wherein the operation stopping device stops operation of the read-only second port of the multi-port memory when the identical address detection device determines that the input address to the readable and writeable first port and the input address to the read-only second port are identical, and a writing operation to the first port is enabled; and

a selector device,

wherein the selector device selects data and outputs data on the readable and writeable first port of the multi-port memory when the identical address detection device determines that the input address to the readable and writeable first port and the input address to the read-only second port are identical, and a writing operation to the first port is enabled.

16. An arbiter device according to claim 15, wherein the selector device selects data and outputs data on the read-only second port of the multi-port memory when the identical address detection device determines that the input address to the readable and writeable first port and the input address to the read-only second port are not identical, and a writing operation to the first port is enabled.

17. An arbiter device according to claim 15, wherein identical address detection device is responsive to at least one of the input address to the readable and writeable first port and the input address to the read-only second port.

18. An arbiter device according to claim 15, wherein identical address detection device is adapted to generate an identical address detection signal if the input address to the readable and writeable first port and the input address to the read-only second port are identical.

19. An arbiter device according to claim 15, wherein the selector device is responsive to at least one of a data output signal of the readable and writeable first port, a data output signal of the read-only second port, and a buffer output signal.

20. An arbiter device according to claim 15, wherein the selector device is adapted to generate a data output signal.

21. An arbiter device according to claim 15, wherein the arbiter device arbitrates between accesses to the readable and writeable first port and the read-only second port.

22. A semiconductor device , comprising:

a multi-port memory equipped with a first port and a second port;

an identical address detection device,

wherein the identical address detection device determines that an input address to the first port and an input address to the second port are identical;

an operation stopping device,

wherein the operation stopping device stops operation of the second port when the identical address detection device detects that the input address to the first port and the input address to the second port are identical ; and

a selector device,

wherein the selector device selects data and outputs data on the first port when the identical address detection device determines that the input address to the first port and the input address to the second port are identical.

23. An arbiter device according to claim 22, wherein the selector device selects data and outputs data on the second port when the identical address detection device determines that the input address to the first port and the input address to the second port are not identical.

24. An arbiter device according to claim 22, wherein identical address detection device is responsive to at least one of the input address to the first port and the input address to the second port.

25. An arbiter device according to claim 22, wherein identical address detection device is adapted to generate an identical address detection signal if the input address to the first port and the input address to the second port are identical.

26. An arbiter device according to claim 22, wherein the selector device is responsive to at least one of a data output signal of the first port, a data output signal of the second port, and a buffer output signal.

27. An arbiter device according to claim 22, wherein the selector device is adapted to generate a data output signal.

28. An arbiter device according to claim 22, wherein the arbiter device arbitrates between accesses to the first port and the second port.

29. A semiconductor device, comprising:

a multi-port memory equipped with a write-only first port and a read-only second port;

an identical address detection device,

wherein the identical address detection device determines that an input address to the first port and an input address to the second port are identical ;

an operation stopping device,

wherein the operation stopping device stops an operation of the second port when the identical address detection device detects that the input address to the first port and the input address to the second port are identical; and

a selector device ,

wherein the selector device selects data and outputs data on the first port when the identical address detection device determines that the input address to the first port and the input address to the second port are identical.

30. An arbiter device according to claim 29, wherein the selector device selects data and outputs data on the second port when the identical address detection device determines that the input address to the first port and the input address to the second port are not identical.

31. An arbiter device according to claim 29, wherein identical address detection device is responsive to at least one of the input address to the first port and the input address to the second port.

32. An arbiter device according to claim 29, wherein identical address detection device is adapted to generate an identical address detection signal if the input address to the first port and the input address to the second port are identical.

33. An arbiter device according to claim 29, wherein the selector device is responsive to at least one of a data output signal of the first port, a data output signal of the second port, and a buffer output signal.

34. An arbiter device according to claim 29, wherein the selector device is adapted to generate a data output signal.

35. An arbiter device according to claim 29, wherein the arbiter device arbitrates between accesses to the first port and the second port.

36. A semiconductor device, comprising:

a multi-port memory equipped with a readable and writeable first port and a read-only second port;

an identical address detection device,

wherein the identical address detection device determines that an input address to the first port and an input address to the second port are identical and a writing operation to the first port is enabled;

an operation stopping device,

wherein the operation stopping device stops an operation of the second port when the identical address detection device detects that the input address to the first port and the input address to the second port are identical and the writing operation to the first port is enabled ; and

a selector device,

wherein the selector device selects data and outputs data on the first port when the identical address detection device determines that the input address to the first port and the input address to the second port are identical and the writing operation to the first port is enabled.

37. An arbiter device according to claim 36, wherein the selector device selects data and outputs data on the second port when the identical address detection device determines that the input address to the first port and the input address to the second port are not identical and the writing operation to the first port is enabled.

38. An arbiter device according to claim 36, wherein identical address detection device is responsive to at least one of the input address to the first port and the input address to the second port.

39. An arbiter device according to claim 36, wherein identical address detection device is adapted to generate an identical address detection signal if the input address to the first port and the input address to the second port are identical.

40. An arbiter device according to claim 36, wherein the selector device is responsive to at least one of a data output signal of the first port, a data output signal of the second port, and a buffer output signal.

41. An arbiter device according to claim 36, wherein the selector device is adapted to generate a data output signal.

42. An arbiter device according to claim 36, wherein the arbiter device arbitrates between accesses to the first port and the second port.